EAST SEARCH

6/21/2007

L#	Hits	Search String	Databases
S1	12	very long instruction word with simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S2	77	very long instruction word same simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S3	1929	very long instruction word with processor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S4	1951	S2 or S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S5	55	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S6	13	S4 and (simulat$3 with ((group or set or plurality) near2 instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S7	408	S4 and simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S9	59	S7 and (simulat$3 with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S10	32	S7 and (simulat$3 with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S12	4	S7 and (generat$3 with simulat$3 with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S27	6	very long instruction word with processor with resource	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S11	2	S7 and (simulat$3 with cycle-by-cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S28	17	S7 and (stor$3 with "register set")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S13	0	S7 and (generat$3 with instuction with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S14	2	S7 and (display$3 with simulat$3 with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S33	4	S7 and ((count$3 or number) with (execution near2 cycle))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S35	3	S7 and (cancel$3 with execution)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S16	1	S7 and (simulat$3 with stop with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S17	1	S7 and (break with condition with stop)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S18	50	S7 and (simulat$3 with pipeline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S19	12	S7 and (simulat$3 with (simultaneous$2 or concurrent$2))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S20	2	S7 and (display$3 with pipeline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S21	102	S7 and (pipeline with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S22	43	S7 and (pipeline with stage)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S23	9	S7 and (simulat$3 with step with execution)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S24	10	S7 and (step with execution with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S47	12	S44 and S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S25	7	S7 and (step with execution with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S26	2	S7 and (step with execution with display$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S29	14	S7 and ((reconstruct$3 or creat$3 or generat$3) with resource)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S8	2	S7 and (simulat$3 with instruction-by-instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S30	102	S7 and ((sav$3 or stor$3) with (memory near2 (data or writing)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S31	3	S7 and (break with condition with determin$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S32	10	S7 and ((updat$3 or chang$3) with resource)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S36	25	S7 and (delay$3 with (cycle or insruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S37	137	S7 and (updat$3 with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S34	3	S7 and (cancel$3 with execution with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S39	218	S7 and ((updat$3 or delay) with (information or instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S38	4	S7 and (output near2 dependency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S41	162	S1 or S2 or S5 or S6 or S8 or S9 or S10 or S11 or S12 or S14 or S15 or S16 or S17 or S18 o	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S40	183	S7 and ((updat$3 or delay) with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

S42	304	S21 or S30 or S37 or S40 or S39	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S43	142	S41 and S42	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S44	162	S41 or S43	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S45	13	S44 and S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S46	0	S7 and (simulat$3 with instruction-based)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S15	3	S7 and (break with condition with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S49	77	very long instruction word same simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S54	408	S51 and simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S59	4	S54 and (generat$3 with simulat$3 with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S60	2	S54 and (display$3 with simulat$3 with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S51	1952	S49 or S50	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S50	1930	very long instruction word with processor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S58	2	S54 and (simulat$3 with cycle-by-cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S55	2	S54 and (simulat$3 with instruction-by-instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S68	43	S54 and (pipeline with stage)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S48	12	very long instruction word with simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S75	14	S54 and ((reconstruct$3 or creat$3 or generat$3) with resource)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S57	32	S54 and (simulat$3 with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S61	3	S54 and (break with condition with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S53	13	S51 and (simulat$3 with ((group or set or plurality) near2 instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S52	55	S49 and S50	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S64	50	S54 and (simulat$3 with pipeline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S65	12	S54 and (simulat$3 with (simultaneous$2 or concurrent$2))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S56	59	S54 and (simulat$3 with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S62	1	S54 and (simulat$3 with stop with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S80	3	S54 and (cancel$3 with execution with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S63	1	S54 and (break with condition with stop)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S66	2	S54 and (display$3 with pipeline)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S93	5	S51 and (pipeline with cycle with (simulat$3 or debug$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S67	102	S54 and (pipeline with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S70	10	S54 and (step with execution with instruction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S101	28	S99 or S100	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S71	7	S54 and (step with execution with cycle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S69	9	S54 and (simulat$3 with step with execution)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S73	6	very long instruction word with processor with resource	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S72	2	S54 and (step with execution with display$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S90	162	S87 or S89	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S94	8	S51 and (pipeline with instruction with (simulat$3 or debug$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S74	17	S54 and (stor$3 with "register set")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S98	18	S96 or S97	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S76	102	S54 and ((sav$3 or stor$3) with (memory near2 (data or writing)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S77	3	S54 and (break with condition with determin$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S78	10	S54 and ((updat$3 or chang$3) with resource)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S79	4	S54 and ((count$3 or number) with (execution near2 cycle))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S82	25	S54 and (delay$3 with (cycle or insruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S81	3	S54 and (cancel$3 with execution)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S83	137	S54 and (updat$3 with result)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S84	4	S54 and (output near2 dependency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

S86	183	S54 and ((updat$3 or delay) with instruction)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S85	218	S54 and ((updat$3 or delay) with (information or instruction))		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S87	162	S48 or S49 or S52 or S53 or S55 or S56 or S57 or S58 or S59 or S60 or S61 or S62 or S63 c		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S88	304	S67 or S76 or S83 or S86 or S85		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S89	142	S87 and S88		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S95	12	S51 and (((group or multiple or plurality) near2 instruction) with (simulat$3 or debug$4))		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S91	325	S51 and (pipeline with cycle)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S92	419	S51 and (pipeline with instruction)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S96	18	S93 or S94 or S95		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S97	17	S96 and (S87 or S88)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S99	5	S91 and (cycle with debug$4)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S100	28	S92 and (instruction with debug$4)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S103	28	S101 or S102		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S102	11	S101 and (S87 or S88)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S105	2	S104 and (simultaneous$2 near2 execut$3)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S104	2		20040117172	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S106	0	S104 and ((simultaneous$2 near2 execut$3) with (different near2 stage))		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S107	1	S104 and ((simultaneous$2 near2 execut$3) with stage)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S109	1	S108 and (stor$3 with data)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S108	2		20010025363	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S127	32	S126 and ((simulate or simulated or simulating or simulation) with (result or output))		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S118	87	very long instruction word same (simulate or simulated or simulating or simulation)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S110	2202	very long instruction word with processor		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S124	55	S120 and ((simulate or simulated or simulating or simulation) with instruction)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S128	90	S126 or S127		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S121	12	S120 and (parallel near2 pipeline)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S120	419	S119 and (simulate or simulated or simulating or simulation)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S123	39	S120 and (pipeline near2 stage)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S125	36	S120 and ((simulate or simulated or simulating or simulation) with cycle)		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S126	90	S121 or S123 or S124 or S125		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S119	2229	S110 or S118		US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

10730120 **Kohsaku Shibata**

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Results of search set S91:

Document Kind Code	Title	Issue Date	Current OR	Abstract
US 20060174059 A1	Speculative data loading using circular addressing or simulated circular addressing	20060803	711/110	
US 20060150170 A1	Methods and apparatus for automated generation of abbreviated instruction set and configur	20060706	717/158	
US 20060107158 A1	Functional coverage driven test generation for validation of pipelined processors	20060518	714/741	
US 20060095750 A1	Processes, circuits, devices, and systems for branch prediction and other processor improver	20060504	712/240	
US 20060095745 A1	Processes, circuits, devices, and systems for branch prediction and other processor improver	20060504	712/238	
US 20060095716 A1	Super-reconfigurable fabric architecture (SURFA): a multi-FPGA parallel processing architect	20060504	712/24	
US 20060075285 A1	Fault processing for direct memory access address translation	20060406	714/5	
US 20060067436 A1	Metacores: design and optimization techniques	20060330	375/341	
US 20060047776 A1	Automated failover in a cluster of geographically dispersed server nodes using data replicatio	20060302	709/217	

US 20060015855 A1	Systems and methods for replacing NOP instructions in a first program with instructions of a s	20060119	717/136
US 20050289259 A1	Methods and apparatus for providing bit-reversal and multicast functions utilizing DMA contro	20051229	710/72
US 20050262510 A1	Multi-threaded processing design in architecture with multiple co-processors	20051124	718/105
US 20050223253 A1	Methods and apparatus for power control in a scalable array of processor elements	20051006	713/322
US 20050216702 A1	Dual-processor complex domain floating-point DSP system on chip	20050929	712/35
US 20050189976 A1	Enhanced negative constraint calculation for event driven simulations	20050901	327/175
US 20050182916 A1	Processor and compiler	20050818	712/24
US 20050172050 A1	Methods and apparatus for providing data transfer control	20050804	710/22
US 20050166039 A1	Programmable event driven yield mechanism which may activate other threads	20050728	712/227
US 20050162456 A1	Printer with capacitive printer cartridge data reader	20050728	347/19
US 20050151777 A1	Integrated circuit with tamper detection circuit	20050714	347/19
US 20050149697 A1	Mechanism to exploit synchronization overhead to improve multithreaded performance	20050707	712/214
US 20050149693 A1	Methods and apparatus for dual-use coprocessing/debug interface	20050707	712/34
US 20050086653 A1	Compiler apparatus	20050421	717/151
US 20050086040 A1	System incorporating physics processing unit	20050421	703/22
US 20050075849 A1	Physics processing unit	20050407	703/2
US 20050075154 A1	Method for providing physics simulation data	20050407	463/1
US 20050055389 A1	Method, apparatus and instructions for parallel data conversions	20050310	708/204
US 20050038936 A1	Methods and apparatus for providing bit-reversal and multicast functions utilizing DMA contro	20050217	710/22
US 20050027973 A1	Methods and apparatus for scalable array processor interrupt detection and response	20050203	712/233
US 20050010743 A1	Multiple-thread processor for threaded software applications	20050113	712/10
US 20040268051 A1	Program-directed cache prefetching for media processors	20041230	711/137
US 20040218048 A1	Image processing apparatus for applying effects to a stored image	20041104	348/207.2
US 20040172524 A1	Method, apparatus and compiler for predicting indirect branch target addresses	20040902	712/239
US 20040163083 A1	Programmable event driven yield mechanism which may activate other threads	20040819	718/102
US 20040162925 A1	Methods and apparatus for providing data transfer control	20040819	710/22
US 20040154002 A1	System & method of linking separately compiled simulations	20040805	717/135
US 20040153634 A1	Methods and apparatus for providing context switching between software tasks with reconfigu	20040805	712/228
US 20040117172 A1	Simulation apparatus, method and program	20040617	703/22
US 20040103193 A1	Response time and resource consumption management in a distributed network environment	20040527	709/224
US 20040093484 A1	Methods and apparatus for establishing port priority functions in a VLIW processor	20040513	712/216
US 20040088462 A1	Interrupt control apparatus and method	20040506	710/261
US 20040078674 A1	Methods and apparatus for generating functional test programs by traversing a finite state mc	20040422	714/33
US 20040068701 A1	Boosting simulation performance by dynamically customizing segmented object codes based	20040408	716/4
US 20040065738 A1	Data distribution mechanism in the form of ink dots on cards	20040408	235/454
US 20040060018 A1	Defect tracking by utilizing real-time counters in network computing environments	20040325	716/4
US 20040054871 A1	Methods and apparatus for initiating and resynchronizing multi-cycle SIMD instructions	20040318	712/22
US 20040025073 A1	Method for transforming behavioral architectural and verification specifications into cycle-bas	20040205	713/400
US 20040015931 A1	Methods and apparatus for automated generation of abbreviated instruction set and configura	20040122	717/158
US 20040008327 A1	Image printing apparatus including a microcontroller	20040115	355/18
US 20040008262 A1	Utilization of color transformation effects in photographs	20040115	348/207.2
US 20040008261 A1	Print roll for use in a camera imaging system	20040115	348/207.2
US 20030226120 A1	Metacores: design and optimization techniques	20031204	716/1
US 20030204819 A1	Method of generating development environment for developing system LSI and medium whic	20031030	716/1
US 20030188299 A1	Method and apparatus for simulation system compiler	20031002	717/141
US 20030182539 A1	Storing execution results of mispredicted paths in a superscalar computer processor	20030925	712/225
US 20030171907 A1	Methods and Apparatus for Optimizing Applications on Configurable Processors	20030911	703/14
US 20030154349 A1	Program-directed cache prefetching for media processors	20030814	711/137

US 20030079065 A1	Methods and apparatus for providing data transfer control	20030424	710/22
US 20030040898 A1	Method and apparatus for simulation processor	20030227	703/21
US 20030040896 A1	Method and apparatus for cycle-based computation	20030227	703/13
US 20030037305 A1	Method and apparatus for evaluating logic states of design nodes for cycle-based simulation	20030220	716/4
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US 5925123 A	Processor for executing instruction sets received from a network or from a local memory	19990720	712/212
US 5896521 A	Processor synthesis system and processor synthesis method	19990420	703/21
US 5832205 A	Memory controller for a microprocessor for detecting a failure of speculation on the physical r	19981103	714/53
US 5313551 A	Multiport memory bypass under software control	19940517	711/149
JP 2003345606 A	METHOD, PROGRAM, AND APPARATUS FOR SIMULATION	20031205	

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US 20040117172 A	Simulation apparatus for very long instruction word processor, generates simulation result of	20040617
JP 2003345606 A	Processor command execution simulation method in digital consumer-application apparatus,	20031205
JP 2002304292 A	Simulation method of very long instruction word processor, involves decoding basic comman	20021018

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L#	Hits	Search String	Databases
L1	1046	very long instruction word with processor	US-PGPUB
L2	51	very long instruction word same (simulate or simulated or simulating or simulation)	US-PGPUB
L3	1062	1 or 2	US-PGPUB
L4	236	3 and (simulate or simulated or simulating or simulation)	US-PGPUB
L5	5	4 and (parallel near2 pipeline)	US-PGPUB
L6	17	4 and (pipeline near2 stage)	US-PGPUB
L7	30	4 and ((simulate or simulated or simulating or simulation) with instruction)	US-PGPUB
L8	21	4 and ((simulate or simulated or simulating or simulation) with cycle)	US-PGPUB
L9	44	5 or 6 or 7 or 8	US-PGPUB
L10	10	9 and (parallel.CLM.)	US-PGPUB
L11	5	9 and (pipeline.CLM.)	US-PGPUB
L12	14	9 and (cycle.CLM.)	US-PGPUB
L13	25	10 or 11 or 12	US-PGPUB
L16	1	9 and (instruction-by-instruction.CLM.)	US-PGPUB
L14	1	9 and (cycle-by-cycle.CLM.)	US-PGPUB

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US 20070078640 A1	Performance simulation of multiprocessor systems	20070405	703/21	
US 20070050682 A1	Processor and debugging device	20070301	714/45	
US 20060095750 A1	Processes, circuits, devices, and systems for branch prediction and other processor improvei	20060504	712/240	
US 20060095745 A1	Processes, circuits, devices, and systems for branch prediction and other processor improvei	20060504	712/238	
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US 20050189976 A1	Enhanced negative constraint calculation for event driven simulations	20050901	327/175	
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US 20050075849 A1	Physics processing unit	20050407	703/2	
US 20050075154 A1	Method for providing physics simulation data	20050407	463/1	
US 20050027973 A1	Methods and apparatus for scalable array processor interrupt detection and response	20050203	712/233	
US 20040172524 A1	Method, apparatus and compiler for predicting indirect branch target addresses	20040902	712/239	

US 20040154002 A1	System & method of linking separately compiled simulations	20040805	717/135
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US 20040093484 A1	Methods and apparatus for establishing port priority functions in a VLIW processor	20040513	712/216
US 20040088462 A1	Interrupt control apparatus and method	20040506	710/261
US 20040025073 A1	Method for transforming behavioral architectural and verification specifications into cycle-bas	20040205	713/400
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